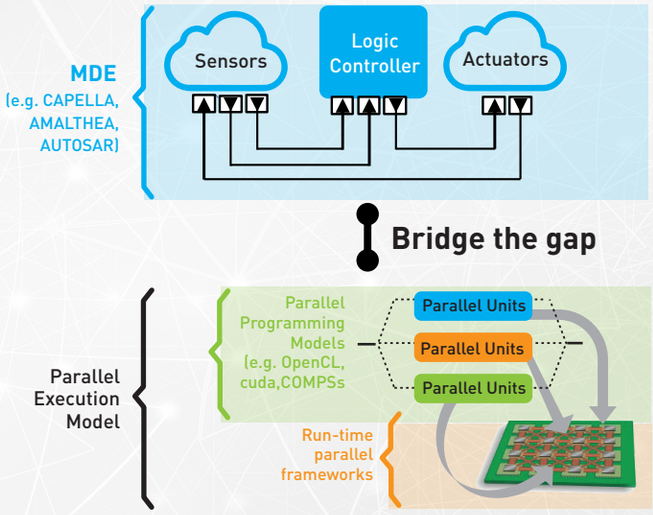
WHAT IS IT?

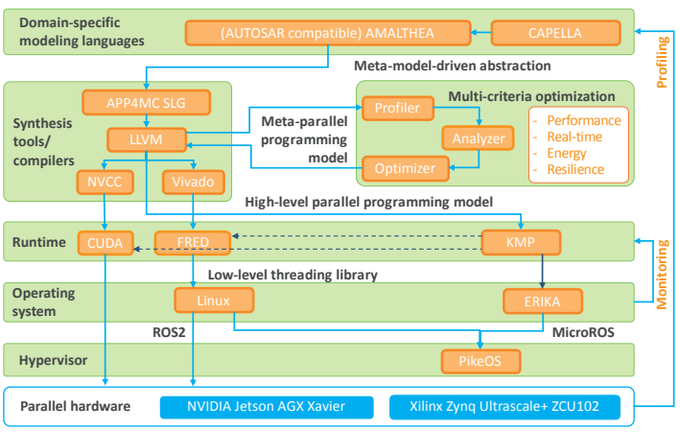
An innovation software architecture that helps unleash the efficient use of parallel and heterogeneous processor architectures for automotive and railway systems, by bridging the gap between model driven engineering and HPC parallel programming models.



WHY AMPERE?

It provides solutions for system integrators and end-users who need to incorporate energy-efficiency and parallel computing into their cyber physical systems.

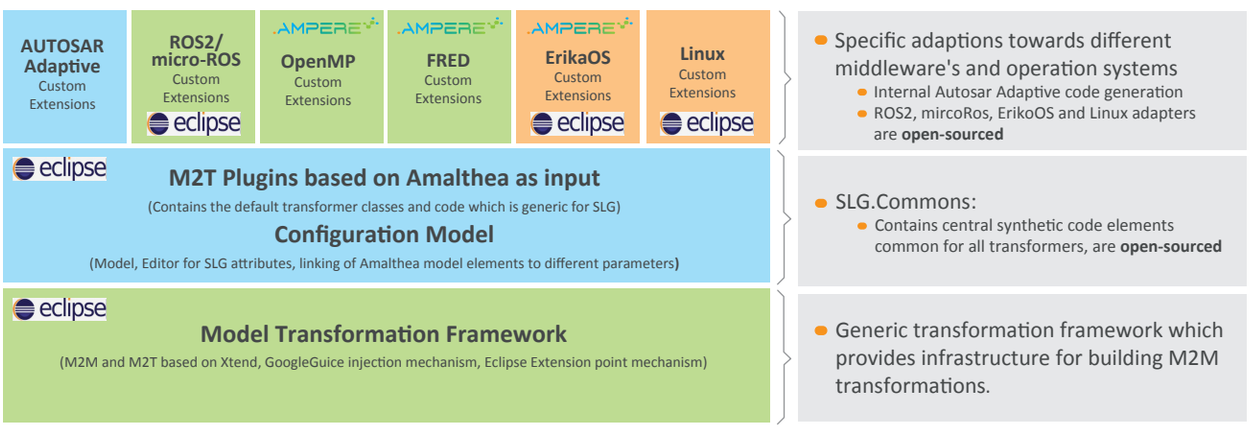
The AMPERE SW architecture includes



1 **Two Domain Specific Modeling Languages (DSML),** i.e., Capella and Amalthea, that facilitate the description of the functional and non-functional behaviour of the system, independently of the underlying platform. The DSMLs have been extended with new features to better describe its parallel nature and its non-functional requirements

2 A **set of synthesis tools** integrated within the APP4MC framework capable of automatically transforming the DSML describing the system to parallel source code supporting:

- OpenMP parallel programming model and dynamic partial reconfiguration FPGA bitstreams
- ROS and MicroROS frameworks to communicate between hypervisor partitions



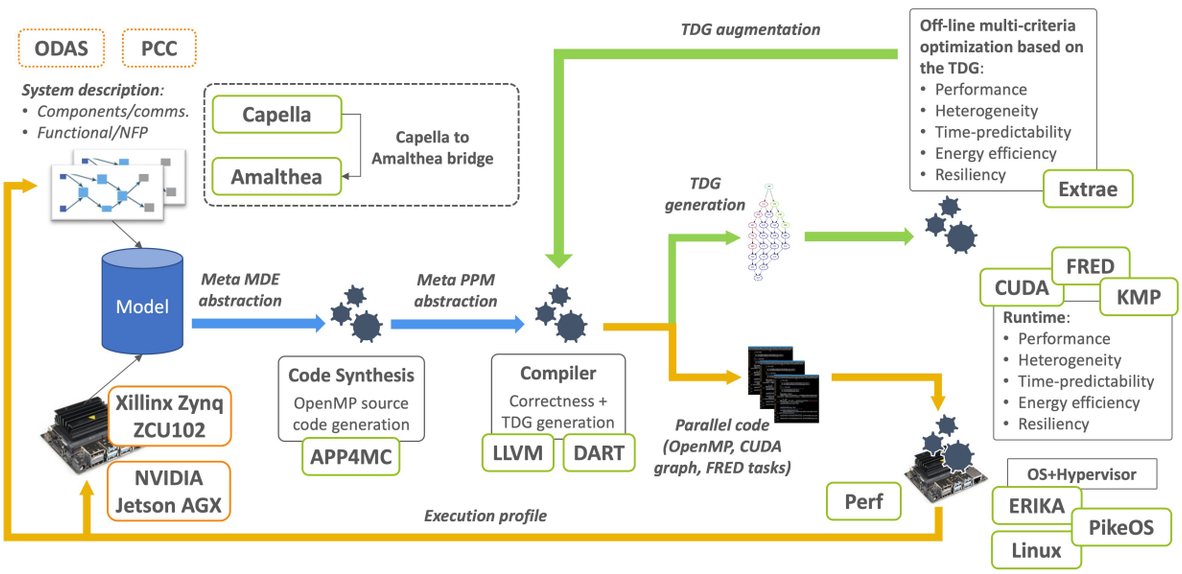
3 **An extended OpenMP programming language** to support very fine-grain parallelism and Redundant execution to enhance system resiliency, by taking benefit of the parallel capabilities the underlying platform

4 A set of **compiler analysis tools,** implemented on top of the LLVM upstream capable of extracting the parallel structure of the system described with the DSML in the form of a task dependency graph or TDG

5 **A multi-criteria analysis tool** to characterise the timing and energy behaviour of the transformed OpenMP program from the DSML description, based on the information provided by the and included into the TDG.

6 A **run-time environment** that constantly monitors time and energy, and adapts the execution to better fulfil the non-functional requirements and a **hypervisor and operating systems** to provide safety and security mechanisms, while supporting the OpenMP parallel execution model.

The AMPERE SW architecture implements the complete value chain for the development, deployment and efficient execution of cyber-physical systems, guaranteed the non-functional requirements imposed by the system



KEY ACHIEVEMENTS:

- Reduction of 30% on the software development costs, while providing the required performance and energy budget imposed by system
- Up to 3x of performance speed-up and a system utilization of 100% for the two AMPERE use cases, guaranteeing the fulfilment of the non-functional requirements
- Provide extensions for automotive and railway DSMLs to better capture requirements
- New extensions to the OpenMP parallel programming framework targeting cyber-physical systems

AMPERE USE-CASES

Predictice cruise control

- Extends Adaptive Cruise Control with data from the electronic horizon to improve fuel efficiency
- Showcases the increased composition and integration capabilities of the AMPERE framework

Obstacle Detection and Avoidance System (ODAS)

ADAS functionalities (i.e., obstacle detection and collision avoidance based on data coming from tam sensors and AI analytics